On page 2 of the Office Action, claims 18-37 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,677,224 (Kadosh). The Examiner states:

> Kadosh et al. shows (FIG. 1U) a semi-conductor device including a plurality of field effect transistors, each transistor comprising a gate (130) over a channel and a deep source (206) and drain (198) region with dopants of a first conductivity type (P). Source (204) and drain (152) extension regions are integral with the deep source and drain regions, respectively. The source extension is more heavily doped (P+) than the drain extension (P-). Kadosh shows all of the elements of the claims except the drain extension being deeper than the source extension. Kadosh does disclose that the source extension is deeper than the drain extension such that the device has a low source-drain series resistance and reduced hot carrier effects. Therefore, it would have been an obvious modification to one of ordinary skill in the art to form the drain extension deeper than the source extension to lower the drain-source series resistance since a drain and source are made of the same materials and only differ because of biasing of the circuit. With respect to the limitations of the claims concerning the specific depth and concentration of the dopants, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dopants at a specific depth and concentration, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

Applicant respectfully traverses the rejection. Kadosh is referred to below as the cited art.

Applicant respectfully traverses the Examiner's contention that "it would have been an obvious modification to one of ordinary skill in the art to form the drain extension deeper than the source extension." The Examiner's contention is rooted in a belief that the source and drain region are interchangeable.

Contrary to the Examiner's contention, the source and drain are the distinct structures which have established meanings to one of ordinary skill in the art. Applicant notes that the IEEE Standard Dictionary of Electrical and

Electronics Terms defines the drain as "a region in the device structure of an insulated-gate-field-effect transistor (IGFET) which contains a terminal into which charge carriers flow from the source through the channel. It has the potential which is more attractive than the source for the carriers in the channel." Applicant also notes that the IEEE Standard Dictionary of Electrical and Electronic Terms defines the source as "region in the device structure of an insulated-gate-field-effect transistor (IGFET) which contains the terminal from which charged carrier flow into channel toward the drain. It has the potential which is less attractive than the drain for the carriers in the channel." Therefore, the source and drain have completely distinct functions during the operation of a transistor. In fact, the drain and source have opposite functions as one is a supplier of charge carriers and the other is a receiver of charge carriers. Accordingly, when the invention is related to the specific function of the source and drain, the distinction between the source and drain cannot be ignored.

Each of independent claims 18, 21, and 31 recites a feature in which the drain extension is deeper than the source extension. This structure provides significant advantages. More particularly, the shallower source extension and deeper drain extension achieves at least three beneficial effects: 1. Substantial immunity to short channel effects; 2. reduced peak electric field in the channel region reduced possibility of hot-carrier injection into the gate oxide; and 3. higher drive current. See present application, page 3, lines 1-10. The shallower source extension allows the transistor to achieve control of short channel effects and higher drive currents and yet the deeper drain extension allows the transistor to reduce hot carrier injection stress. See present application, page 5, line 15 – page 6 – line 7.

Kadosh does not disclose or suggest the structure recited cited in independent claims 18, 21 and 31. Indeed, Kadosh shows a drain extension which is shallower than the source extension. There is no suggestion in Kadosh to exchange the source extension with the drain extension. Not only does Kadosh not provide a suggestion for the structure in the present application, it

teaches precisely the opposite structure. Therefore, claim 18 and its dependent claims 19-20, claim 21 and its dependent claims 22-30 and claim 31 and its dependent claims 32-37 are patentable over the cited art.

As shown in Figure IU, both transistors of Kadosh have a drain extension that is shallower than the source extension. There is clearly no suggestion for the opposite structure recited in the claims 18, 21 and 31 because no where in Kadosh does it mention that the source and the drain extension are interchangeable. Indeed, the specification of Kadosh lists a myriad of alternatives and not one of the alternatives mentions a substitution of the drain extension and the source extension. Kadosh, Col. 10, lines 4-60. Accordingly, claim 18 and its dependent claims 19-20, claim 21 and its dependent claims 22-30 and claim 31 and its dependent claims 32-37 are patentable over the cited art.

Further, although Kadosh mentions the advantages of lower source drain resistance and reduced hot carrier effects, it achieves these advantages by relying on a structure with a lightly doped drain, a heavily doped deep drain and ultra-heavily doped deep source. Kadosh, Col. 3, lines 9-15. If one of ordinary skill in the art used Kadosh in pursuit of the advantages mentioned by the Examiner, that person would fabricate an asymmetric transistor with a heavily doped deep drain and an ultra-heavily doped deep source. Reducing the depth of source extension would not even be considered, especially when Kadosh clearly shows a deeper drain extension. Accordingly, claim 18 and its dependent claims 19-20, claim 21 and its dependent claims 22-30 and claim 31 and its dependent claims 32-37 are patentable over the cited art.

Yet further, rather than relying on ultra-heavy doping of a deep source region, the transistor recited in independent claims 18, 21, and 31 achieves significant advantages with a more elegant structure, a shallower source extension and a deeper drain extension. Achieving advantages with a structure of reduced complexity is strong indicia of nonobviousness. Accordingly, claim 18 and its dependent claims 19-20, claim 21 and its dependent claims 22-30 and claim 31 and its dependent claims 32-37 are patentable over the cited art.

Further, dependent claims 19 and 20 recite a feature wherein the source extension is more heavily doped than the drain extension. Assuming for the sake of argument only that the Examiner's contention the source and drain extension are readily interchangeable to meet the limitations in the claims of the present application, Kadosh would disclose the opposite structure as claimed in claim 19. In claim 19, the source extension, the shallower extension, is more heavily doped than the drain extension, the deeper extension. In contrast, Kadosh clearly shows that the deeper extension is more heavily doped. The Examiner must provide a suggestion in Kadosh to make the shallower extension more heavily doped, especially since such a feature is in contrast to conventional wisdom in which deeper exteriors are more heavily doped. Therefore, Kadosh clearly is teaching the opposite of the structure recited in claims 19 and 20. Accordingly, claims 19 and 20 are additionally patentable over the cited art.

With respect to dependent claim 26, the ratio of dopants between the source extension and the drain extension is recited as being approximately five. In contrast, Kadosh discloses a concentration of ratio of 10 to 100 times. See Kadosh, Col. 3, lines 29-33. Clearly, the ratio of doping is different than that as claimed in dependent claim 26. Further, there is no suggestion to reduce the doping ratio of Kadosh by ½ or less. Accordingly, it is respectfully submitted that claim 26 is patentable over the cited art.

Further, claim 36 has been amended to recite the unique concentration of dopants associated with the deep source and drain regions and the source extension and the drain extension. As discussed above, Kadosh teaches the use of a deep source region having a different concentration of dopants than the deep drain region and the deep source region having a higher concentration of dopants than the drain extension. In contrast, claim 36 recites that the deep source and drain regions have the same dopant concentrations. Further, the range of concentrations recited in claim 36 for the deep source extension is outside of the range disclosed in Kadosh. There is simply no suggestion for

147 altering the concentration of dopants in Kadosh to meet the limitations of claim
148 36. Accordingly, claim 36 is patentable over Kadosh.

149 Applicant believes that the present application is now in condition for
150 allowance. Favorable reconsideration of the application as amended is
151 respectfully requested. The Examiner is invited to contact the undersigned by
152 telephone if it is felt that a telephone interview would advance the prosecution
153 of the present application.

Respectfully submitted,

Date 12-13-11

By _____

FOLEY & LARDNER
Firstar Center
777 East Wisconsin Avenue
Milwaukee, Wisconsin 53202-5367
Telephone: (414) 297-5768
Facsimile: (414) 297-4900

Joseph N. Ziebert
Attorney for Applicant
Registration No. 35,421

VERSION WITH MARKINGS SHOWING CHANGES

31. An ultra-large scale integrated circuit including a plurality of field effect transistors, the field effect transistors comprising:

a gate structure on a top surface of a semiconductor substrate;

a source extension with dopants of a first conductivity type;

a drain extension with dopants of the first conductivity type; and

[forming] deep source and drain regions with dopants of the first conductivity type, wherein the gate structure is between the source and drain regions, wherein the drain extension is deeper than the source extension.

32. The integrated circuit of claim 31, [wherein the forming source and drain regions] further comprising [comprises]:

[providing] a pair of spacers abutting lateral sides of the gate structure[; and providing a deep source/drain implant at the source location and the drain location].

36. The integrated circuit of claim 31, wherein the [first conductivity type is N-type] deep source and deep drain regions have a concentration of dopants between 10^{19} and 10^{20} dopants per cc, the source extension has a concentration of dopants between $5X10^{19}$ and 10^{20} dopants per cc, and the drain extension has a concentration of dopants between $1X10^{19}$ and $5X10^{19}$ dopants.

37. The integrated circuit of claim 31, wherein the first conductivity type is P-type or N-type.